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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,532	11/29/2001	Scott C. Glenn	42390P12946	5479

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EXAMINER	
CHEN, ALAN S	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 09/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,532	GLENN, SCOTT C.	
	Examiner	Art Unit	
	Alan S Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22 and 27-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23-26* is/are allowed.

6)☒ Claim(s) *1-22 and 27-34* is/are rejected.

7)☒ Claim(s) *2-5 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Words "down" and loadable" on page 1, line 8 should be concatenated.

Space between the word "DATA" and number "2" on pages 4 and 5

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1 and 6 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "channel" in claims 1 and 6 is used by the claims to mean "storage element", while the accepted meaning is "a conduit for data and communications." The term is indefinite because the specification does not clearly redefine the term.

5. Claims 2-5 and 7-9 are rejected as being dependent upon a base claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 6-8, 18 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by No. 5,901,074 to Nakano et al. (hereafter Nakano).

In reference to Claim 1, Nakano discloses an apparatus, comprising:

A storage register (Fig. 1, element 14a) to store first and second data values;

A channel to store data (Fig. 1, element 14b);

Hexadecimal and octal data to be transferred from the channel storage (Fig. 1, element 14b) based on the value of the display register (Fig. 1, element 14a). It is inherent that somewhere along the data path, at least four terminals are present for hexadecimal data, since hex requires a minimum of four binary digits to represent one hex number and four binary digits lines equate to four signal lines. Select lines will be present to change between hex and octal base values (e.g., when either $12d_2$ or $12d_4$ is selected).

In reference to Claim 6, Nakano discloses a device, comprising:

A storage register to store a data field value (Fig 1, element 14a);

A channel to store data (Fig. 1, element 14b); and

Data terminals to provide data from the channel having a base value determined by the data field value (Fig. 1, element 14a).

In reference to Claim 7 and 8, Nakano discloses the device of claim 6 wherein hexadecimal and octal data is transferred from the channel storage (Fig. 1, element 14b) based on the value of the display register (Fig. 1, element 14a). It is inherent that somewhere along the data path, at least four terminals are present for hexadecimal data, since hex requires a minimum of four binary digits to represent one hex number and four binary digits lines equate to four signal lines. The same argument applies for octal numbers. Select lines will be present to change between hex and octal base values (e.g., when either $12d_2$ or $12d_4$ is selected).

In reference to Claim 18 and 19, Nakano discloses a method comprising:

Writing a data bit of a data field (Fig. 1, element 14);

Storing data in a storage device (Fig. 1, element 14b);

Providing the store data at data terminals in a first set of terminals (it is inherent terminals exist between Fig. 1, element 14 and element 11) and depending on the data being transferred, some terminal pins will not be active on both the transmit and receive side (Fig. 1, element 11 and 14).

8. Claims 10, 11, 16, 17, 27 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by No. 5,663,734 to Krasner.

In reference to Claim 10, Krasner discloses a system, comprising:

A first processor (Fig. 1A, element 26) having a first set of terminals for outbound data and a second set of terminals for inbound data (Fig. 1A, element 25, 33 and 35) and a register having a data field to determine the terminals in the first set that provide outbound data (inside microprocessor, Fig. 1A, element 26);

SRAM (Fig. 1A, element 30) coupled to the first processor; and

A second processor (Fig. 1A, element 32) having a first set of terminals for inbound data and coupled to the first set of terminals of the first processor (Fig. 1A, element 33), and a second set of terminals for outbound data and coupled to the second set of terminals of the first processor (Fig. 1A, element 33).

In reference to Claim 11, Krasner discloses a system of claim 10, further a register in the second processor having a data field to determine the terminals in the second set that provide outbound data (inside DSP, Fig. 1A, element 32).

In reference to Claims 16 and 17, Krasner discloses the system of claim 10, wherein the first processor is an applications processor (Fig. 1A, element 26) and the second processor is a baseband processor (Fig. 1A, element 32).

In reference to Claims 27 and 32, Krasner discloses a method and an article that comprise and result in:

transferring data from an application processor (Fig. 1A, element 32) to a baseband processor (Fig. 1A, element 26) through a first set of data pins (Fig. 1A, element 33); and

transferring data from the baseband processor to the applications processor through a second set of data pins (Fig. 1A, element 33).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 12-15, are rejected under 35 USC 103(a) as being unpatentable over Krasner in view of Nakano in further view of Xilinx.

Krasner discloses the system of claim 10.

Krasner does not disclose expressly the system of claim 10 further comprising a channel in the first or second processor to supply or receive outbound or inbound data at the first or second set of terminals based on if it is hexadecimal or octal format specified by the data field.

Nakano discloses a system with the ability to select the data format, whether it is binary, octal or hexadecimal (Fig. 1, element 12).

Xilinx discloses an FPGA that can serve as a processor, with its pinout specified (Table 1). In particular, the clock out can be seen in Table 1 denoted as CCLK. Furthermore, eight data lines, which can be used to represent hexadecimal, octal, or binary number representations is seen in Table 1, denoted as D0-D7, capable of sending out octal or hexadecimal data through the respective data line terminals based a data field inside the processor.

Krasner, Nakano and Xilinx are analogous art because they are from the similar problem solving area in current implementations of processors.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the Xilinx FPGA to implement the processors described by Krasner with the selectable format by Nakano.

The suggestion/motivation for doing so would have been to use current programmable processor technology to implement DSP systems such as the one described by Krasner in addition to having a selectable number representation due to the availability of a plurality of data lines in the FPGA.

Therefore, it would have been obvious to combine Krasner, Nakano and Xilinx for the benefit of using current digital technology and selectable formats.

11. Claims 28-31, 33 and 34 are rejected under 35 USC 103(a) as being unpatentable over Krasner in view of Nakano in further view of Xilinx.

Krasner discloses a method and an article of Claims 27 and 32.

Krasner does not disclose expressly programming a register in the application or baseband processor to select data pins from the first set of data pins to provide hexadecimal, octal or binary data. Furthermore, Krasner does not disclose expressly transferring a clock signal from each processor to the other processor.

Nakano discloses a system with the ability to select the data format, whether it is binary, octal or hexadecimal (Fig. 1, element 12).

Xilinx discloses an FPGA that can serve as a processor, with its pinout specified (Table 1). In particular, the clock out can be seen in Table 1 denoted as CCLK. Furthermore, eight data lines, which can be used to represent hexadecimal, octal, or binary number representations is seen in Table 1, denoted as D0-D7.

Krasner, Nakano and Xilinx are analogous art because they are from the similar problem solving area in current implementations of processors.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to define the numbering system one desires for a digital system, in particular hexadecimal, octal or binary format as specified by Nakano. In the case of Xilinx, one can have two hexadecimal numbers, two octal numbers, or eight binary numbers at each clock cycle. Since there are three number representations to select from, at least two bits are required to select which data pins to group. It would be obvious to one of ordinary skill in the art to define these two bits in a register field due to the small storage space required.

The suggestion/motivation for doing so would have been to provide synchronous transfer of data between processors (for the case of sending a clock to and from processors) and defining the digital number representation to use by the processors.

Therefore, it would have been obvious to combine Krasner, Nakano and Xilinx for the benefit of synchronous data transfer and a selectable number representation.

Allowable Subject Matter

12. Claims 23-26 are allowed.

The following is the statement of reasons for the indication of allowable subject matter: The prior art disclosed by the applicant and cited by the Examiner fail to teach or suggest, alone or in combination, a method comprising selecting a subset of data terminals from a group of data terminals to supply data and supplying a clock from one terminal and supplying a strobe signal from a second terminal and providing data at the selected data terminals when the strobe signal is inactive, the data changing in accordance with the clock signal.

13. Claims 2-5 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is the statement of reasons for the indication of allowable subject matter: The prior art disclosed by the applicant and cited by the Examiner fail to teach or suggest, alone or in combination, an apparatus of claim 1 further comprising a terminal to provide a strobe signal, wherein an identity of the channel is provided at the first thru fourth terminals during the strobe signal; a terminal to receive a wait signal wherein hex or octal data is not changed with the clock signal when the wait signal is received.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to selectable formats and dual processor communication:

U.S. Pat. No. 5,960,035 to Sridhar et al.

U.S. Pat. No. 5,982,807 to Snell

U.S. Pat. No. 6,016,143 to Heinzman

U.S. Pat. No. 6,148,420 to Schlater et al.

U.S. Pat. No. 6,154,785 to Lakhat et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S Chen whose telephone number is 703-605-0708. The examiner can normally be reached on M-F 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

asc
9/9/2003

JEFFREY GAFFIN
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